CLAIMS

What is claimed is:

1. A wide bandwidth phase-lock loop circuit, comprising:

a frequency detector arranged to detect frequency information of an input signal;

a frequency range selector connected to the frequency detector; and

a phase-locked loop connected to the frequency range selector and capable of operating in a plurality of frequency ranges, wherein the frequency range selector configures the phase-locked loop to generate an output signal within one of the plurality of frequency ranges based on the frequency information of the input signal.

2. The circuit of claim 1, further comprising a divider connected to the phase-locked loop and configurable to divide a frequency of the output signal generated by the phase-locked loop.

3. The circuit of claim 1, wherein the frequency range selector employs frequency range hysteresis.

4. The circuit of claim 1, wherein the frequency detector comprises a zero-crossing synchronizer that synchronizes the input signal to a clock signal.

5. The circuit of claim 1, wherein the frequency detector comprises a zero-crossing counter that counts zero-crossings of the input signal.

6. The circuit of claim 1, wherein the frequency range selector comprises a range detector for detecting which one of the plurality of frequency ranges is an appropriate frequency range based on the frequency information of the input signal.

7. The circuit of claim 6, wherein the frequency range selector further comprises a range selector for confirming the frequency range detected by the range detector.

8. The circuit of claim 1, further comprising a voltage comparator connected to the frequency detector and adapted to condition a wave form of the input signal.

9. A method of phase locking a signal having a wide range of frequencies, comprising:

obtaining frequency information of an input signal;

selecting one out of a plurality of frequency ranges based on the frequency information of the input signal; and

generating an output signal within the selected frequency range.

10. The method of claim 9, further comprising dividing a frequency of the output signal.

11. The method of claim 9, further comprising employing frequency range hysteresis.

12. The method of claim 9, further comprising confirming the selected frequency range.

13. The method of claim 9, further comprising synchronizing the input signal to a clock signal.

14. The method of claim 9, further comprising counting zero-crossings of the input signal.

15. The method of claim 9, further comprising conditioning a wave form of the input signal.

16. A phase-lock loop circuit having a wide bandwidth, comprising:

means for obtaining frequency information of an input signal;

means for selecting one out of a plurality of frequency ranges based on the frequency information of the input signal; and

means for generating an output signal in the selected frequency range.

17. The circuit of claim 16, further comprising means for dividing a frequency of the output signal.

18. The circuit of claim 16, wherein the means for selecting employs frequency range hysteresis.

19. The circuit of claim 16, wherein the means for selecting confirms the selected frequency range.

20. The circuit of claim 16, wherein the means for obtaining synchronizes the input signal to a clock signal.

21. The circuit of claim 16, wherein the means for obtaining counts zero-crossings of the input signal.

22. The circuit of claim 16, further comprising means for conditioning a wave form the input signal.

23. A wide bandwidth phase-lock loop circuit, comprising:

a frequency detector arranged to detect frequency information of an input signal, the frequency detector having a zero-crossing synchronizer for synchronizing the input signal to a clock signal and a zero-crossing counter for counting zero-crossings of the input signal;

a frequency range selector connected to the frequency detector and having a range detector and a range selector, wherein the range detector detects which one of a plurality of frequency ranges is an appropriate frequency range based on the frequency information of the input signal, and wherein the range selector confirms the frequency range detected by the range detector;

a phase-locked loop connected to the frequency range selector and configured by the frequency range selector to generate an output signal in the frequency range detected by the range detector, wherein the frequency range selector employs frequency range hysteresis;

a divider for dividing a frequency of the output signal; and

a voltage comparator for conditioning a wave form of the input signal.